Amendments to the Specification:

Please replace paragraph [0003] and [0024] with the following amended paragraphs:

[0003] A PCI/ PCI-X bridge may support multiple concurrent delayed transactions if there are multiple ~~I/O~~ I/O devices or a single I/O device with multiple read requests. In addition, the bus frequency may vary depending on system configurations. The PCI bus can operate at frequencies of 33 MHz or 66 MHz. The PCI-X bus can operate at frequencies of 66 MHz, 100 MHz, or 133 MHz. At these various frequencies, the number of read delayed transactions may be different which affect the depth of the delayed transaction buffer. Existing techniques for buffer management are inefficient. One technique uses a single large content addressable memory (CAM) delayed transaction buffer to support multiple delayed transactions. This technique requires a complex buffer management scheme and is costly. Another technique uses multiple delayed transaction buffers that are deep enough to handle the highest PCI/ PCI-X bandwidth and lowest system latency. This technique requires high gate count and wastes hardware when used with lower bus frequencies.

[0024] The data steering circuit 210 provides the input and output data paths to the primary bus 195 as input and the peripheral secondary PCI/PCI-X bus 185 as output. The data steering circuit 210 is dynamically configured according to the frequency of the peripheral secondary bus 185. In addition, although the invention is described in terms of a delayed transaction read request from the ~~I/O~~ I/O device to the memory, the concept can be readily applied or extended to similar situations where a dynamically configured buffering is needed. This includes a buffered write, a buffered read, etc. The data steering circuit 210 includes a control circuit 212, a dynamically configured input circuit 214, and a dynamically configured output circuit 216.